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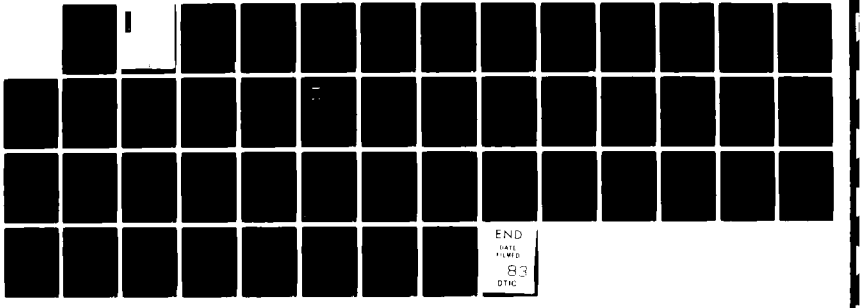

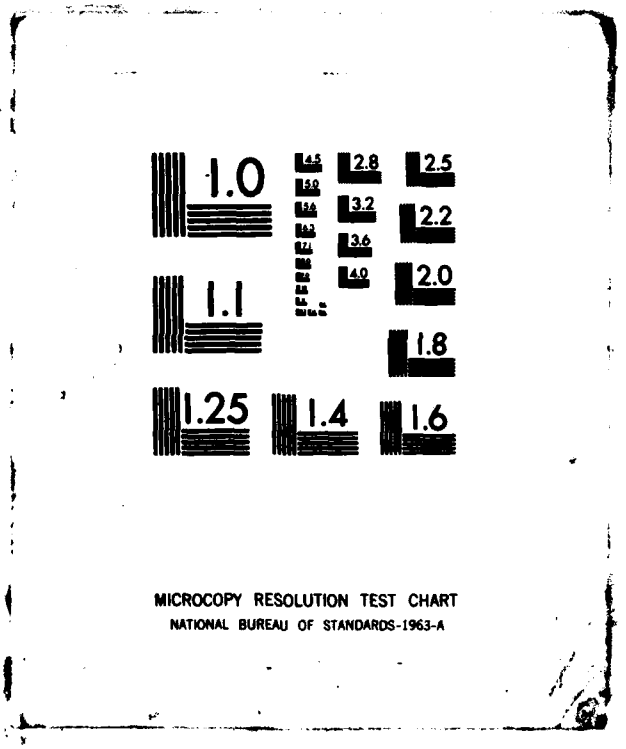
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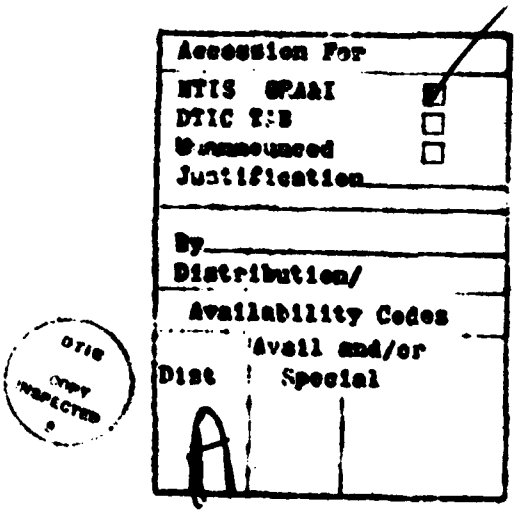

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ANALYSIS OF ELECTRON TRAPS IN SILICON AND GALLIUM ARSENIDE BY DEEP-LEVEL TRANSIENT SPECTROSCOPY

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1. INTRODUCTION

Deep level centers seem to be present in all known semiconductors. They may occur when an impurity is introduced into a crystal or through lattice damage including that caused by various doping methods. One such procedure is ion implantation, where residual damage stems from collisions between the ions and the host atoms, leaving a significant number of dopant atoms interstitially located. Subsequent annealing techniques may be applied to reorder impurity atoms onto active sites.

Deep level centers can be important even in small concentrations due to their ability to significantly limit carrier lifetime as defined by Shockley-Read-Hall statistics (1, 2). The lifetime of excess charge carriers, τ, in a semiconductor with a single impurity level is given by

$$\tau = \frac{c_p(p_0+p_1) + c_n(n_0+n_1)}{c_n c_p N_{TT}(n_0+p_0)} \tag{1.1}$$

where c_n and c_p are the average values of the capture constants of electrons and holes over the states in the bands, n_0 and p_0 are the free-carrier concentrations in thermal equilibrium, n_1 and p_1 are the concentrations of conduction band electrons and valence band holes when the Fermi level (E_F) falls at the impurity level (E_T), and N_{TT} is the number of deep level centers per unit volume. This equation is valid as long as $N_{TT} \ll p_0 + p_1$ and $N_{TT} \ll n_0 + n_1$.

Deep impurity and defect states bring about undesirable trapping effects which may change switching times in devices or non-radiative recombination processes which limit the efficiency of light-emitting diodes. Luminescence (4) has played a major role in the study of impurity and defect

centers. Although it has been used successfully in locating radiative traps, it is only an indirect measure of the presence of non-radiative states. To remedy this, capacitance measurements, a well established technique among experimental physicists (5, 6) for studying energy levels in both insulators and semi-insulating materials can be applied to semiconductors with some modifications. Due to their relatively high conductivity, semiconductors must be examined by using p-n junctions or Schottky barriers in capacitive measurements. The actual probing is of the depletion region which is essentially devoid of mobile carriers, allowing the use of linear rate equations to describe the capture and emission processes (7). Furthermore, though traditional capacitance measurements are carried out on linear dielectrics and employ sinusoidal driving fields, when large forward bias pulses are applied to the depletion region of these non-linear elements, as occurs during trap loading procedures, transient methods prove more advantageous (8).

In 1966, R. Williams (9) was the first to use barrier capacitance to determine the occupation of deep level states within the forbidden gap. By applying a reverse bias to an n-type gallium arsenide (GaAs) Schottky barrier, centers below the Fermi level will ionize in the barrier region (or depletion width for a p-n junction) thereby changing the total concentration of charge. When this occurs, the small signal ac capacitance increases with time until all the centers are ionized. From this change in capacitance, deep center concentration is determined. Subsequent capacitance transient techniques have been applied, most notably to silicon (Si) by Sah (7) as well as to gallium phosphide (10), zinc selenide (11) and zinc telluride (12). Yet, all these methods have lacked either sensitivity, speed, range of observable trap depths or adequate resolution. Such were the target areas when D. V. Lang introduced

deep-level transient spectroscopy (DLTS) in 1974 (13, 14).

Among the important features of DLTS is a fast transient recovery time. Since changes in the charge of a trap and the corresponding change in the junction capacitance is of interest, fast system response will detect traps with slower emission rates. Therefore, intermediate as well as deep traps can be observed with DLTS. This technique also achieves high resolution of signals from different traps, thus providing a practical means of doing spectroscopy on non-radiative centers.

The versatility of DLTS, however, is not limited to detecting radiative and non-ratiative centers of varying depths; it also distinguishes between majority and minority carrier traps and includes the effect of the junction electric field in enhancing thermal emission rates.

The importance of the junction electric field is seen in heavily doped semiconductors where the field can reach 10^5 - 10^6 V/cm and substantially increase emission rates, altering both trap location and profile measurements (15).

The purpose of this work is to compare the effectiveness of swept line electron beam (SLEB) annealing to that of thermal annealing by analyzing deep levels with DLTS. Residual damage will be investigated in both Si and GaAs samples. The results presented in this paper will not reflect junction field dependence.

2. EXPERIMENTAL PROCEDURES

2.1. Ion Implantation

Ion implantation provides doping uniformity, controllability and reproducibility in the doping of semiconductors and thus is a viable alternative to thermal diffusion. A typical implanter, shown schematically in Fig. 2.1, includes an ion source, a mass separator and a target chamber.

Basically, implantation consists of forming a plasma containing the desired ions, accelerating the ions to a high energy, selecting the chosen ions by mass separation and then scanning the ion beam over the sample. In the target chamber, the sample holder is tilted from the beam normal by an angle of 7° so that channeling of ions along specific crystal directions is avoided.

The implanted atoms form a distribution in the substrate which depends on the acceleration voltage, the impurity and the host atom. As the incident ions enter the crystal, they give up their energy through nuclear and core electron collisions. These primary collisions displace host atoms, which in turn are stopped by cascade collision processes at some average penetration depth, called the projected range, R_p.

The distribution of the impurity atoms is approximated by the Lindhard-Schoitt (LSS) theory (16) using a Gaussian function

$$N(x) = \frac{N_D}{\Delta R_p \sqrt{2\pi}} \exp\left[\frac{-(x - R_p)^2}{2\Delta R_p^2}\right] \qquad (2.1)$$

where N_D is the dose (ions/cm^2), R_p is the projected range (cm) and ΔR_p is the projected standard deviation (cm).

This doping method produces lattice damage which results from collisions between the ions and the lattice atoms. In order to restore lattice

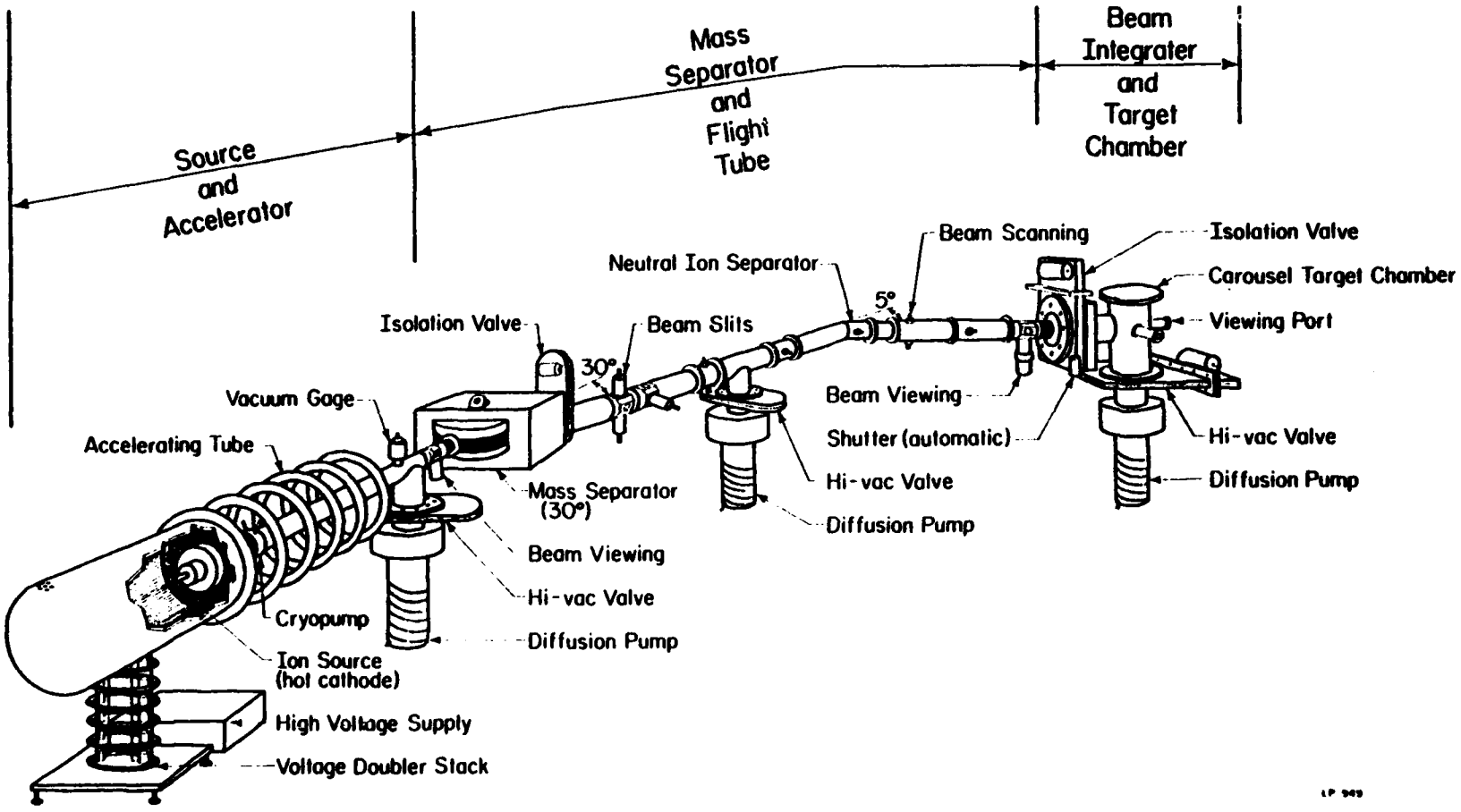


Fig. 2.1. Schematic diagram of the 300 keV ion implantation system.

order, the substrate can be annealed by various methods.

2.2. Silicon Nitride Deposition

In annealing GaAs, it is necessary to encapsulate the sample surface to prevent outdiffusion of the host atoms. In this work, an rf-plasma enhanced reaction of nitrogen with silane is used to deposit a Si_3N_4 film on the sample prior to annealing (17). This method produces nitrides with little oxygen contamination, thereby restricting gallium outdiffusion during the annealing of GaAs (18).

The reactor is shown schematically in Fig. 2.2. After loading the samples onto a graphite heater, the chamber and gas lines are pumped down to 2.7×10^{-4} Pa. A preliminary nitrogen discharge, lasting a few minutes, is initiated to remove remaining oxygen from the system while the sample is covered by a shutter. Nitrogen and silane are then introduced, the shutter is removed, the samples are heated to 330°C and rf-plasma deposition is begun. Typically, 10 to 12 minute discharges deposit 1000 Å Si_3N_4 films.

2.3. Annealing Techniques

2.3.1. Thermal Annealing

Thermal anneals take place in a Trans Temp furnace with flowing forming gas (4.1% H_2 in N_2). The sample temperature is monitored by a chromel-alumel thermocouple and a Fluke 2165A digital thermometer. Generally, anneals are 800° or 900°C for 30 minutes, after which the samples are pulled slowly from the furnace. By pulling the sample tray a few inches every 30 seconds for 3 minutes, the sample temperature drops from 900°C to 400°C before emerging from the furnace. This procedure restores the crystal to an equilibrium state while avoiding quenching.

2.3.2. Swept-Line Electron Beam Annealing

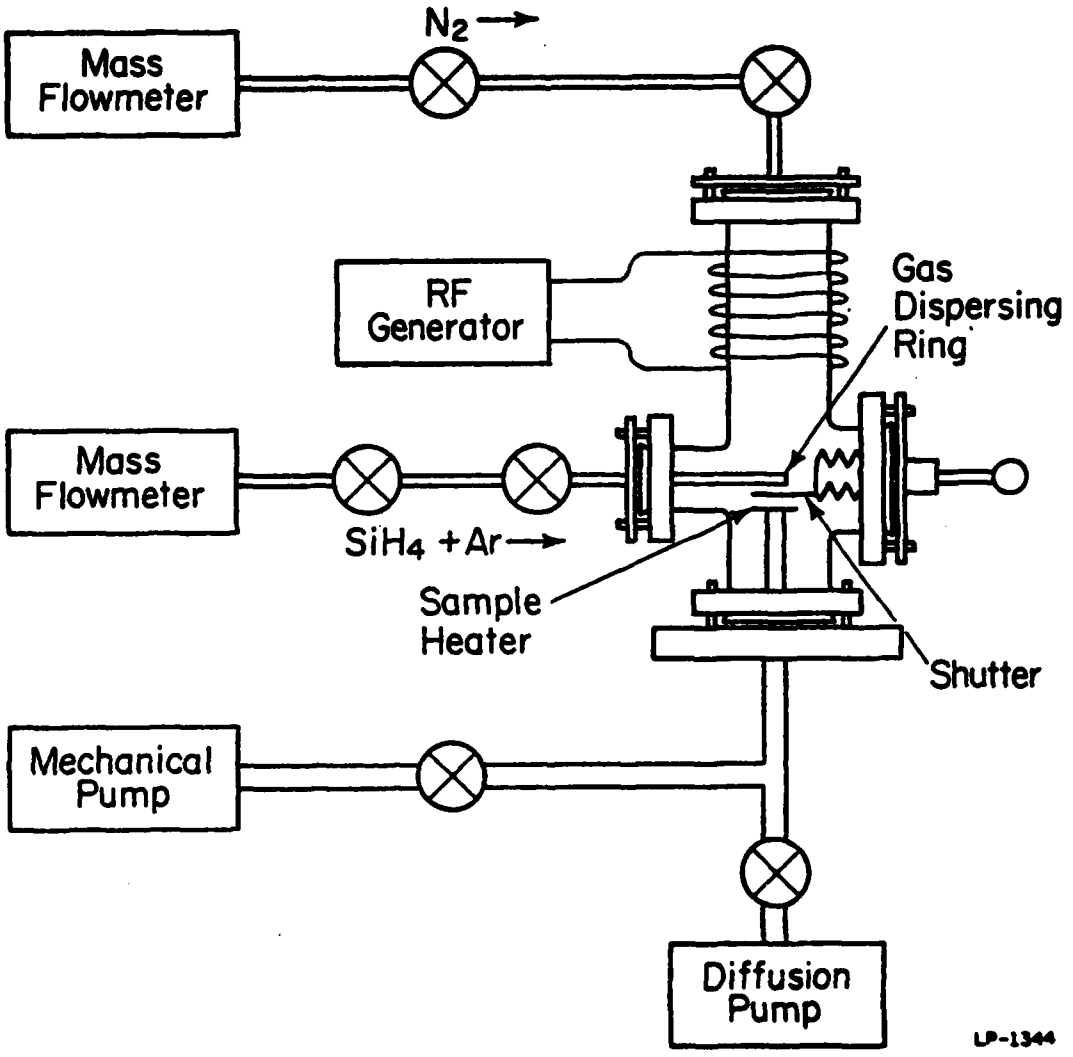


Fig. 2.2. Schematic diagram of the rf-plasma Si_3N_4 deposition system [17].

Swept-line electron beam annealing (SLEB) is performed in a stainless steel vacuum chamber at 1.3×10^{-4} Pa. A schematic diagram of this system is shown in Fig. 2.3. Samples are mounted on a graphite-coated molybdenum plate with a graphite adhesive suspension. This in turn is mounted on a 9-kg copper heat sink which sits on a motor-driven x-y translation table.

The electron gun (General Vacuum Model EBG - 101) is mounted vertically in the chamber and produces a cylindrically symmetric beam with an energy range of 0 to 30 keV. The beam is lengthened when magnetically focused onto a slit. By properly adjusting the slit width, slit height and the magnetic lens focusing voltage, a rectangular spot is produced. To prevent thermal strains, the beam is made sufficiently long to cover the edges of the sample.

The variac which drives the translation table also controls the sweep speed. The speed is determined by scanning the beam over two adjacent Faraday cups with the output registered on a chart recorder. Generally, speeds of 0.5 to 0.6 cm/sec are employed.

The molybdenum plate is preheated to 150 to 160°C. During beam translation, the surface of the sample reaches 800 to 900°C and cools immediately when the pass is completed. Thus, a quenching effect is inherent in this annealing process.

2.4. Device Processing

2.4.1. Silicon

In this study, Schottky barriers are fabricated from 0.24 Ω-cm Czochralski grown bulk silicon, doped with 4×10^{16} cm^{-3} phosphorus. To begin the experiment, a continuous amorphous layer is formed by four cold ($\leq$100°C) Si^+ implants of energies 32, 91, 158 and 255 keV. These energies and the

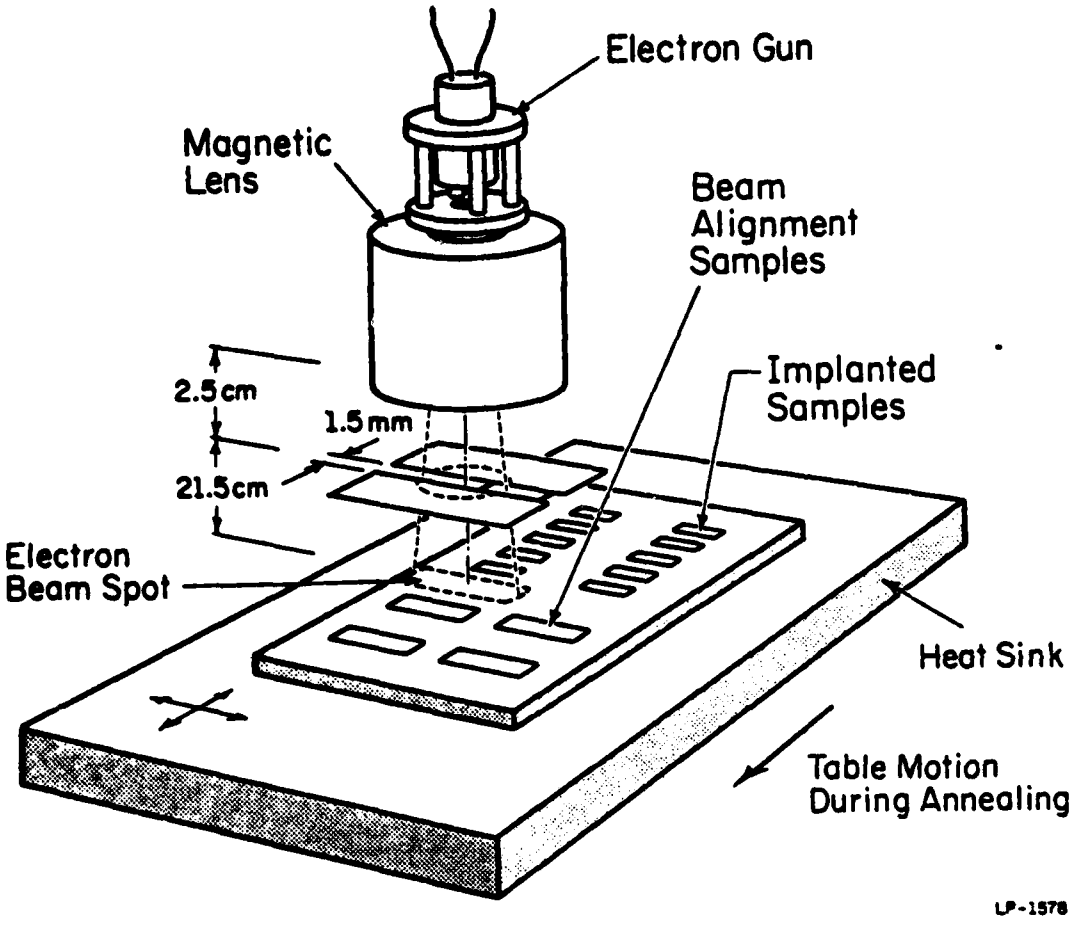


Fig. 2.3. Schematic diagram of the electron beam annealing apparatus [24].

corresponding doses produce an approximately 0.5 μm deep, flat profile of 1 x 10^{20} cm^{-3}. From etching experiments (19), an amorphous depth of 4550 Å ± 125 Å was determined.

The samples are divided into two groups, one for SLEB recrystallization and one for thermal annealing. The SLEB samples are annealed at 20 keV with a table translation speed of 0.32 cm/sec. The second set are made up of samples that have been thermally annealed at either 600, 700 or 800°C for 30 minutes in a quartz-lined furnace tube under forming gas ambient.

After annealing, the surface is anodically oxidized to remove a 200 Å layer of Si, exposing a clean surface. Aluminum is then evaporated onto this surface forming a Schottky barrier and ohmic contacts are evaporated on the back-side. Both evaporations pass through shadow masks to define contacts which are sintered at 350°C for 15 seconds. Two devices with similar C-V and I-V characteristics are mounted on a single TO-18 header, followed by thermocompression lead bonding.

2.4.2. Gallium Arsenide

In this study, samples are fabricated from n-type gallium arsenide (GaAs) grown from a stochiometric melt and doped with Si (8 x 10^{15} cm^{-3}) (20). The fabrication of p-n junctions is shown in Fig. 2.4. Initially, a 1000 Å layer of Si_3N_4 is deposited on clean samples, and the area to be implanted is defined by 10-mil circular openings in a mask made of a 4-μm to 6-μm layer of AZ1350J photoresist (PR). Plasma etching is used to remove the Si_3N_4 from the windows. Room temperature beryllium (Be^+) implants are now performed at 100 keV with a dose of 1 x10^{14} cm^{-2}, creating a junction depth of approximately 0.73 μm. The samples are divided into two groups, those to be SLEB annealed and those to be thermally annealed. The PR is then removed with acetone and another 1000 Å layer of Si_3N_4 is deposited on the top surface of the SLEB

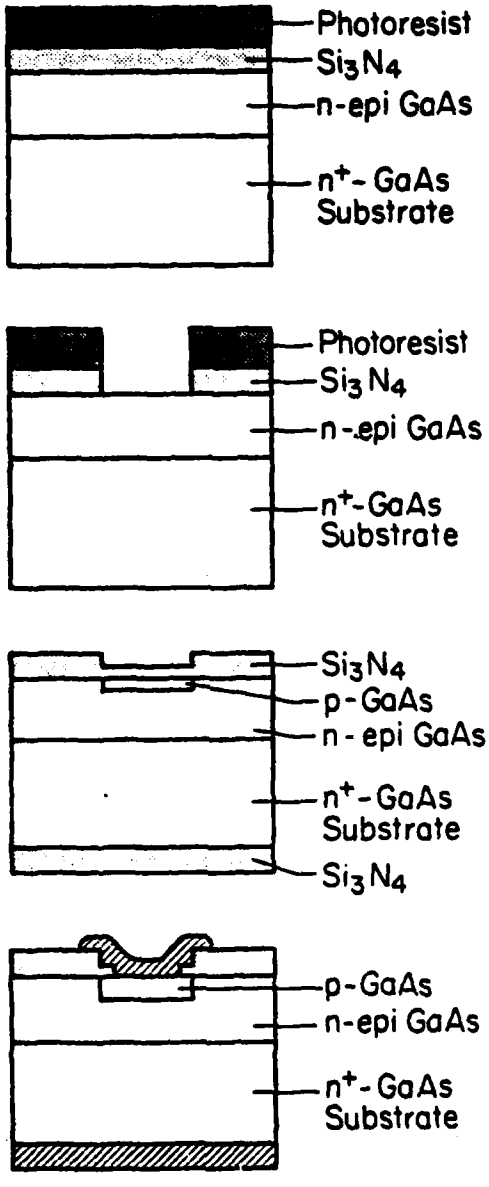


Fig. 2.4. Schematic cross section of GaAs planar diodes at various points in the fabrication procedure.

samples and on the back-side as well for samples to be thermally annealed. The back surface of the SLEB samples need not be coated because of the negligible arsenic loss from this face due to the limited heating time involved in this annealing method. In this case, Si_3N_4 encapsulation prevents As evaporation during annealing, since GaAs tends to dissociate at high temperatures.

The SLEB diodes are annealed at beam energies of 20 to 25 keV and beam currents between 3 and 6 mA with sweep speeds of 0.5 to 0.6 cm/sec. The second group of diodes are thermally annealed for 30 minutes at 800°C or 900°C.

After annealing, the nitride layer is removed from the back-side using a buffered etch containing one part HF and five parts 40% NH_4F solution. Ohmic contacts are then formed on this n-region by evaporating 88% Au -12% Ge alloy and sintering at 450°C for 5 seconds in flowing H_2.

Using the same photolithographic technique as before, 5-mil circular windows are opened over the Be-implanted regions and 96% Au - 4% Mn alloy contacts are formed by evaporation.. The contacts are sintered at 330°C for 5 seconds in flowing H_2. Two diodes, one of each type, are cut and mounted on a single TO-18 header for DLTS measurements and gold-tantalum wires are used to connect the diodes to the header posts.

2.5. Deep-Level Transient Spectroscopy (DLTS)

DLTS (13, 14) is a capacitance transient method for studying deep level impurity and defect centers in semiconductors. This is achieved by monitoring the effect of deep traps on the capture and emission of electrons and holes in the depletion region of a p-n junction or Schottky barrier, where the rate equations can be linearized.

Since DLTS is basically a pulsed junction capacitance transient

technique, such transients will first be described, assuming only a single trap level. These are three major processes by which transitions occur at deep centers i.e., thermal, optical and Auger (7). For simplicity, only the thermal process will be discussed here to illustrate the rate equation.

When transitions take place, trap concentrations increase with electron captures or hole emissions and decrease with electron emissions and hole captures:

$$\frac{dn_T}{dt} = c_n n (N_{TT} - n_T) + e_p (N_{TT} - n_T) - e_n n_T - c_p p n_T \qquad (2.2)$$

where $N_{TT} = n_T + p_T$; n, p represent electron concentration in the conduction band and hole concentration in the valence band, respectively; n_T, p_T are the occupied and empty deep level concentrations, respectively; c_n, c_p are electron and hole capture coefficients; and e_n, e_p are electron and hole emission rates. In the depletion region where $n = p \simeq 0$

$$\frac{dn_T}{dt} = -(e_n + e_p) n_T + e_p N_{TT}$$

and the solution is

$$n_T(t) = N_{TT} \frac{e_p}{e_p + e_n} + N_{TT} \frac{e_n}{e_p + e_n} \exp[-(e_p + e_n)t] \qquad (2.3)$$

where $n_T(0) = N_{TT}$.

At thermal equilibrium, the rate at which electrons are emitted to the conduction band, e_n, can be related to the electron capture coefficient, c_n, and the capture cross section, σ_n, by

$$e_n = c_n N_c g_n \exp[-(E_c - E_T)/k_B T] = \sigma_n \langle v_n \rangle N_c g_n \exp[-(E_c - E_T)/k_B T) \qquad (2.4)$$

Similarly, the rate at which holes are emitted to the valence band, e_p, can be related to the hole capture coefficient, c_p, and the capture cross section,

σ_p, by

$$e_p = c_p N_v g_p \exp[-(E_T - E_v)/k_B T] = \sigma_p \langle v_p \rangle N_v g_p \exp[-(E_T - E_v)/k_B T] \quad (2.5)$$

where N_c, N_v are the effective densities of states in the conduction and valence bands; g_n and g_p are the degeneracy factors of the deep level; $\langle v_n \rangle$, $\langle v_p \rangle$ are the root-mean-square (rms) thermal velocities of free electrons and holes; and k_B is the Boltzmann constant. It is apparent from these equations that emission rates can be used to obtain both capture cross sections and trap energy levels.

The electron traps in Fig. 2.5 are majority carrier traps. Initially, there is a quiescent depletion width, created by a reverse bias across the junction. The depletion region capacitance of this abrupt p^+-n junction on an n-type semiconductor is

$$C = \frac{\epsilon A}{W} = A\sqrt{\frac{\epsilon q N_D^+}{2(V_R + V_{bi})}} \quad (2.6)$$

where V_{bi} is the built-in voltage of the junction; V_R is the reverse bias; ϵ is the semiconductor permittivity; q is the elemental charge; N_D^+ is the density of fixed charge on the n-side (assumed constant in the depletion region); A is the area of the junction; and W is the depletion width. When a forward bias is applied, this region collapses and the electron traps are filled.

Immediately after the trap-filling pulse, carriers in the shallow donor states are thermally excited into the conduction band and are swept away by the junction electric field. The capacitance then decreases to the value contributed by the net ionized donors and the electrons in the trapping centers. Thermal emission of the trapped electrons is a slow process, and the

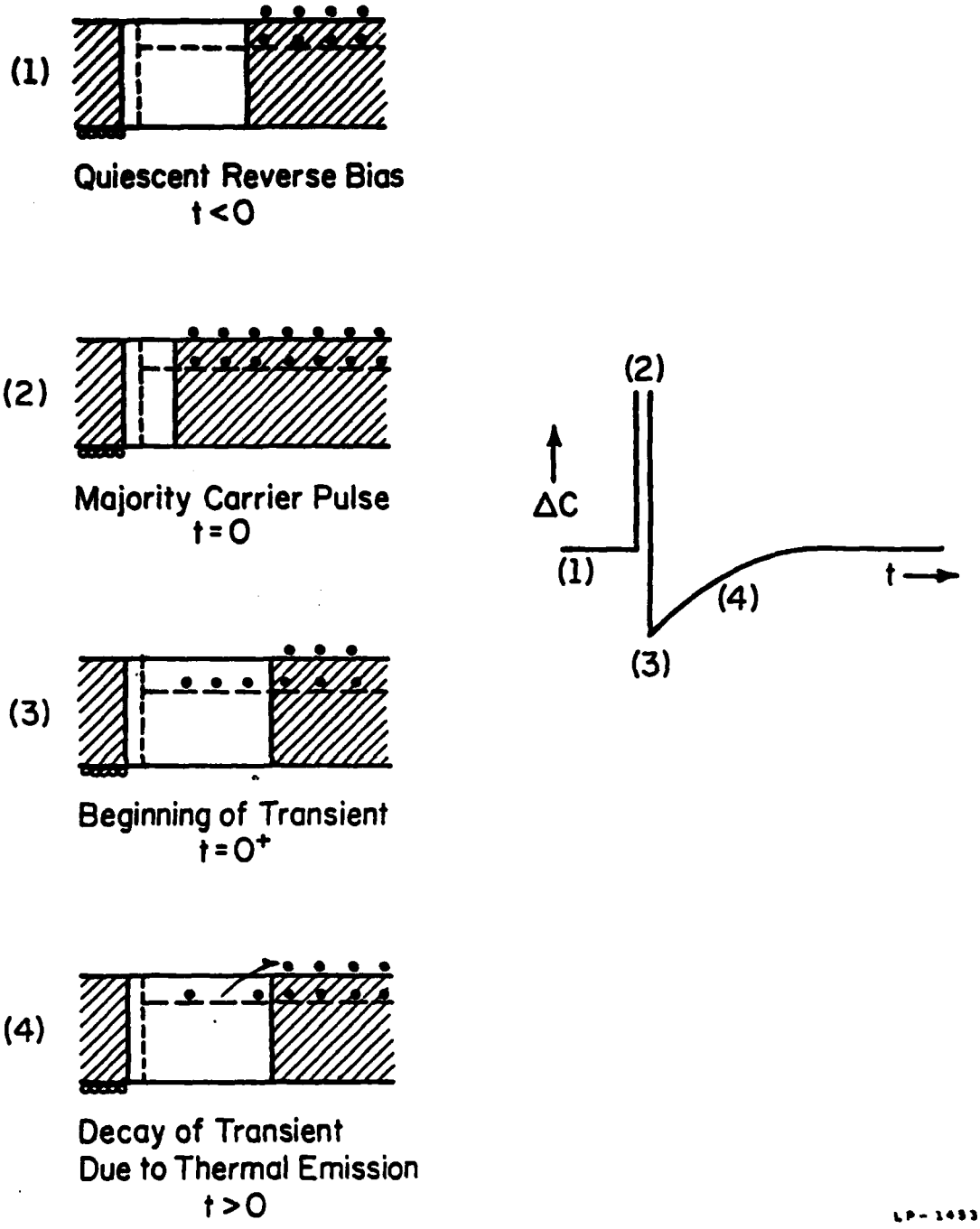


Fig. 2.5. Capacitance transient due to a majority carrier trap in a p^+-n diode. The insets labeled 1 through 4 schematically show the charge state of the defect level and width of the space charge region (unshaded portion) at various times before and during the transient [14].

time constant τ_n ($= 1/e_n$) depends mainly on the ratio of the activation energy to the device temperature. Therefore, a slow capacitance transient can be observed in a suitable temperature range and used to determine various parameters characterizing this deep level. If trapping centers are assumed to be neutral when filled with electrons, then after the pulse, the total charged centers are

$$N^{+} = N_D^{+} + N_{TT}\,(1 - e^{-t/\tau_n}) \tag{2.7}$$

The capacitance transient can be obtained mathematically from

$$C(t) = A\sqrt{\varepsilon q[N_D^{+} + N_{TT}(1 - e^{-t/\tau_n})} \tag{2.8}$$

$$\Delta C = C(\infty) - C(0) = C(\infty)\left[1 - \sqrt{\frac{N_D^{+}}{N_D^{+} + N_{TT}}}\right] \tag{2.9}$$

If $(N_{TT}/N_D^{+}) < 0.1$,

$$C(t) = A\sqrt{\frac{\varepsilon q\, N_D^{+}}{2(V_R + V_{bi})}\,(1 - \tfrac{1}{2}\,\frac{N_{TT}}{N_D^{+}}\,e^{-t/\tau_n})}$$

$$\Delta C(t) = C(\infty) - C(t) = C(\infty)\,\tfrac{1}{2}\,\frac{N_{TT}}{N_D^{+}}\,e^{-t/\tau_n} \tag{2.10}$$

$$\Delta C = \Delta C(0) = C(\infty)\,\tfrac{1}{2}\,\frac{N_{TT}}{N_D^{+}}$$

$$\frac{N_{TT}}{N_D^{+}} = \frac{2\Delta C}{C(\infty)} \tag{2.11}$$

Thus, exact trap concentration in the depletion region can be obtained from ΔC if the density of fixed charge, N_D^{+}, is known.

While the preceding discussion is concerned with a single level,

DLTS is able to separate several deep centers and display these levels as a function of device temperature. This is done by passing the transient through an electronically preset rate window which permits only the trap with an emission rate within the window to be observed by the system. The junction is thermally scanned so that the temperature corresponding to each windowed emission rate and its respective trap can be determined.

The rate window can be set by a dual-channel boxcar averager (see Fig. 2.6) or a lock-in amplifier (21-23). The boxcar averager measures the difference of the capacitance at two sampling instants t_1 and t_2. The boxcar output is thus given by

$$S(\tau) = C(t_1) - C(t_2) = \Delta C(e^{-t_1/\tau} - e^{-t_2/\tau}) \qquad (2.12)$$

the signal $S(\tau)$ will reach a mixiumum at the temperature where the thermal emission τ_{max} is obtained from

$$(dS(\tau)/d\tau)/_{\tau_{max}} = 0 \text{ or } \tau_{max} = (t_2-t_1)/\ln(t_2/t_1).$$

A single thermal scan will display one peak for each deep level in the material.

The devices in this study are scanned from -150°C to +150°C. Then profiling and frequency analysis is performed on each peak to determine the concentration, energy level and capture cross section of each trap.

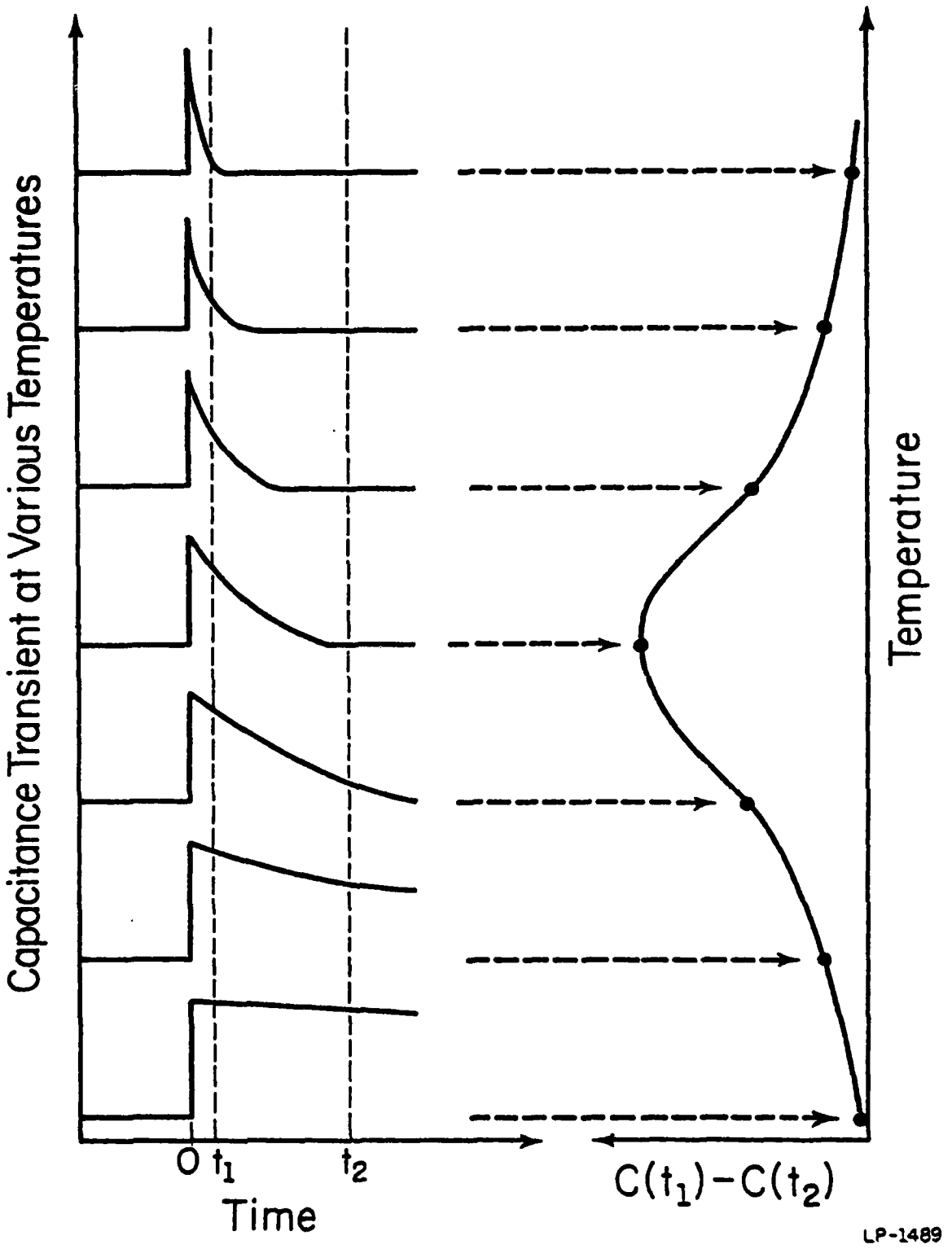
2.5.1. Majority and Minority Carrier Traps

The capacitance transients and the DLTS peaks of majority carrier and minority carrier traps have opposite polarities. Therefore, a DLTS spectrum clearly indicates the type of trapping centers.

2.5.2. Trap Concentration

The DLTS peak is proportional to ΔC, which is related to trap

Fig. 2.6. Illustration of how a dual-channel boxcar averager is used to define the rate window. The left hand side shows capacitance transients at various temperatures, while the right-hand side shows the corresponding DLTS signal resulting from using the boxcar averager to display the difference between the capacitances at times t_1 and t_2 as a function of temperature [14].


Capacitance Transient at Various Temperatures
Temperature
0
t_1
t_2
Time
$C(t_1)-C(t_2)$
LP-1489

concentration by Eq. (2.7). Initially, a scan from 123 K to 432 K is performed with each peak representing a trap. Fig. 2.7 displays a typical scan. When a peak is identified, a conversion factor (V/pF) is determined by taking a voltage reading before and after one picofarad (1 pF) is added to the high sensitivity capacitance bridge used for detecting the capacitance transient. By adding a known capacitance to the bridge and observing its response, an unambiguous calibration is made of the system. ΔC in pF can now be calculated using the following equation:

$$\Delta C = \frac{H \times S \times 0.5 \times 0.565}{F} \tag{2.13}$$

where H is the peak height in cm; S is the sensitivity setting for each peak in volts; 0.5 is the chart vertical sensitivity; 0.565 is a constant resulting from the lock-in amplifier signal processing; and F is the conversion factor. This process is performed for each peak, first with only the quiescent reverse bias applied across the junction and then an additional reducing bias is applied in 1/2 or 1 V increments until the depletion region is completely collapsed. For example, if the quiescent bias is -10 V and measurements are taken in 1/2 V increments, then ΔC's are determined for forward bias' ranging from 0 to +10 V. Fixed capacitance measurements corresponding to each effective voltage (quiescent bias plus reducing bias) are then taken using a Boonton 72B capacitance meter.

The trap concentration profile is given by:

$$N_{TT}(x) = \frac{\delta\left(\frac{\Delta C}{C_q}\right)}{\delta V}\left(\frac{q W^2 N_D^+(W_q)}{\varepsilon}\right) N_D^+(x) \tag{2.14}$$

where W is the depletion width as a function of the effective bias; $N_D^+(W_q)$ is

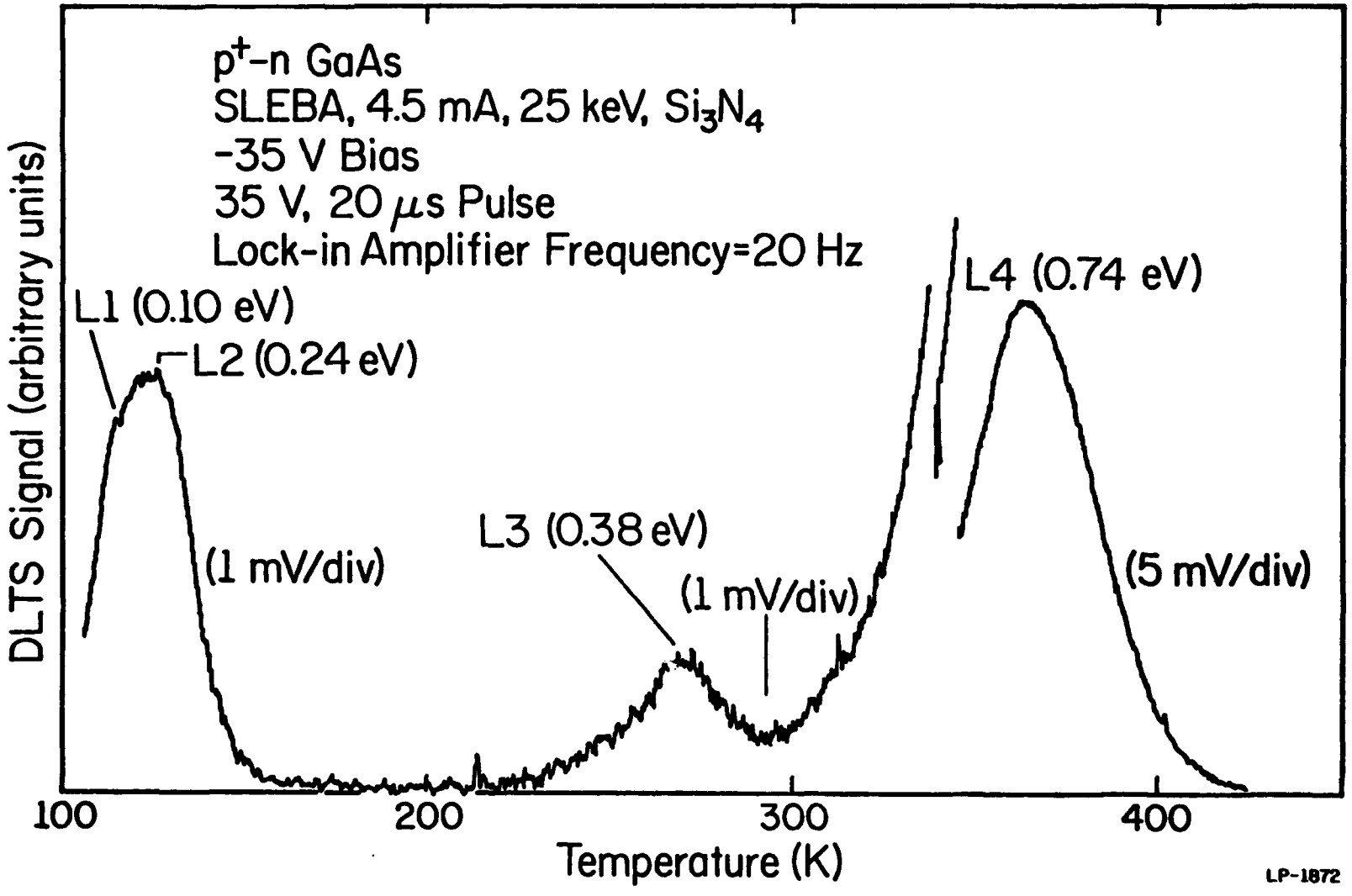


Fig. 2.7. Typical DLTS thermal scan with each peak, L1 through L4, representing a defect level.

the fixed charge concentration at the edge of the depletion region on the n-side when the effective voltage equals the quiescent reverse bias; C_q is the capacitance corresponding to the quiescent bias; W is given by Eq. (2.5); and

$$N_D^+(x) = \frac{C^3}{\varepsilon q A^2 (dC/dV)} \tag{2.15}$$

The trap profile is a function of the space charge region penetration into the n material.

Once $\Delta C/C_q$ is determined, $\delta(\Delta C/C_q)/\delta V$ is computed by averaging the difference between the preceding and the following values of $\Delta C/C_q$ from the point in question. δV is the voltage increments used (in this study, either 0.5 or 1 V). The value of dC/dV in Eq. (2.13) is determined by a similar averaging technique.

2.5.3. Trap Energy Level

Multiphonon emission is a commonly occuring non-radiative mechanism in both GaAs and GaP (25). At sufficiently high temperatures, multiphonon emission causes the capture cross section to increase exponentially with temperature. From this feature, Lang et al. (25, 26) arrived at the following relationship:

$$T^2\tau_n \approx \exp[\Delta E/k_B T] \tag{2.16}$$

Thus, from the preset emission rate windows and the corresponding temperatures of each DLTS peak, an Arrhenius plot of $T^2\tau_n$ vs 1000/T can be obtained. The energy depth, ΔE, is determined from the slope of this plot. With this information, capture cross section can be determined from Eq. (2.3).

In this study, a lock-in amplifier is used to set the rate windows at 10, 20, 50, 100, 200 and 500 Hz. The frequency analysis is performed with

the applied quiescent bias and a reducing bias of equal magnitude. At each setting, a computer records the height and resistance as a single peak is scanned. Calibration data for platinum resistance thermometers are supplied by Rosemont Inc. to determine the temperature corresponding to each DLTS peak. Fig. 2.8 displays a typical scan. The increase in peak height with increasing emission rate window is due in part to field effects (27) or as suggested by Rockett and Peaker (28), to a natural consequence of the change in shape of the Debye tail with temperature.

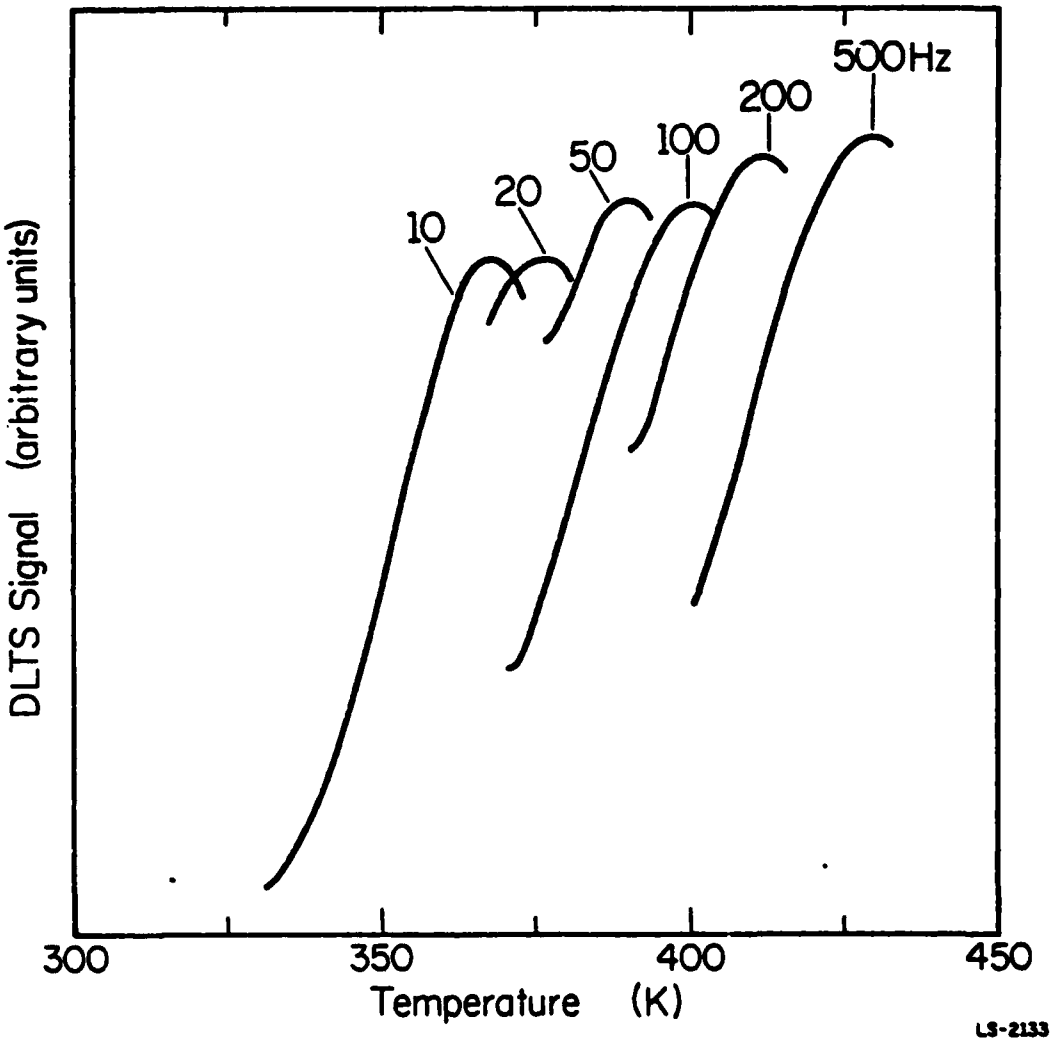


Fig. 2.8. DLTS frequency analysis illustrating temperature dependence of the peak height.

3. RESULTS AND DISCUSSION

3.1. Silicon

DLTS spectra for 30 minute furnace anneals, 600, 700 and 800°C are shown in Fig. 3.1. Two distinct defect signals are observed. The lower temperature signal having an activation energy $\Delta E = 0.22$ eV below the conduction band edge appears in all three cases and becomes dominant as the annealing temperature is increased. The second peak changes from $\Delta E = 0.5$ eV to 0.35 eV to 0.42 eV with increasing temperature. Defects with activation energies with $\pm$ 0.02 eV of these four traps have been observed in implanted (29), irradiated (21, 30) or laser (31) damaged Si.

Similar spectra for SLEB samples at three peak beam power densities is shown in Fig. 3.2. There is a marked reduction in signal height from lowest to highest power densities, the latter ($I_{peak} = 38.0$ W/cm^2) producing peak signals a factor of four smaller than the smallest peak in the 800°C case. The thermal activation energies observed in SLEB samples, with the exception of $\Delta E = 0.34$ eV, do not correspond with those noted in the furnace annealed material. Activation energies within $\pm$ 0.02 eV of $\Delta E = 0.17$, 0.18, 0.34 and 0.4 eV, however, have been previously identified in implanted (29), irradiated (21, 30) or laser (31) damaged Si. The level $\Delta E = 0.80$ eV has not been previously reported.

In regions where the defect concentrations are comparable to that of fixed charge, the fixed charge profile includes not only ionized donors, but defects as well (32). This occurs to some extent in the profile of the 800°C material shown in Fig. 3.3. A large trap concentration appears at 0.45 μm which is near the original amorphous-crystalline interface (indicated by the

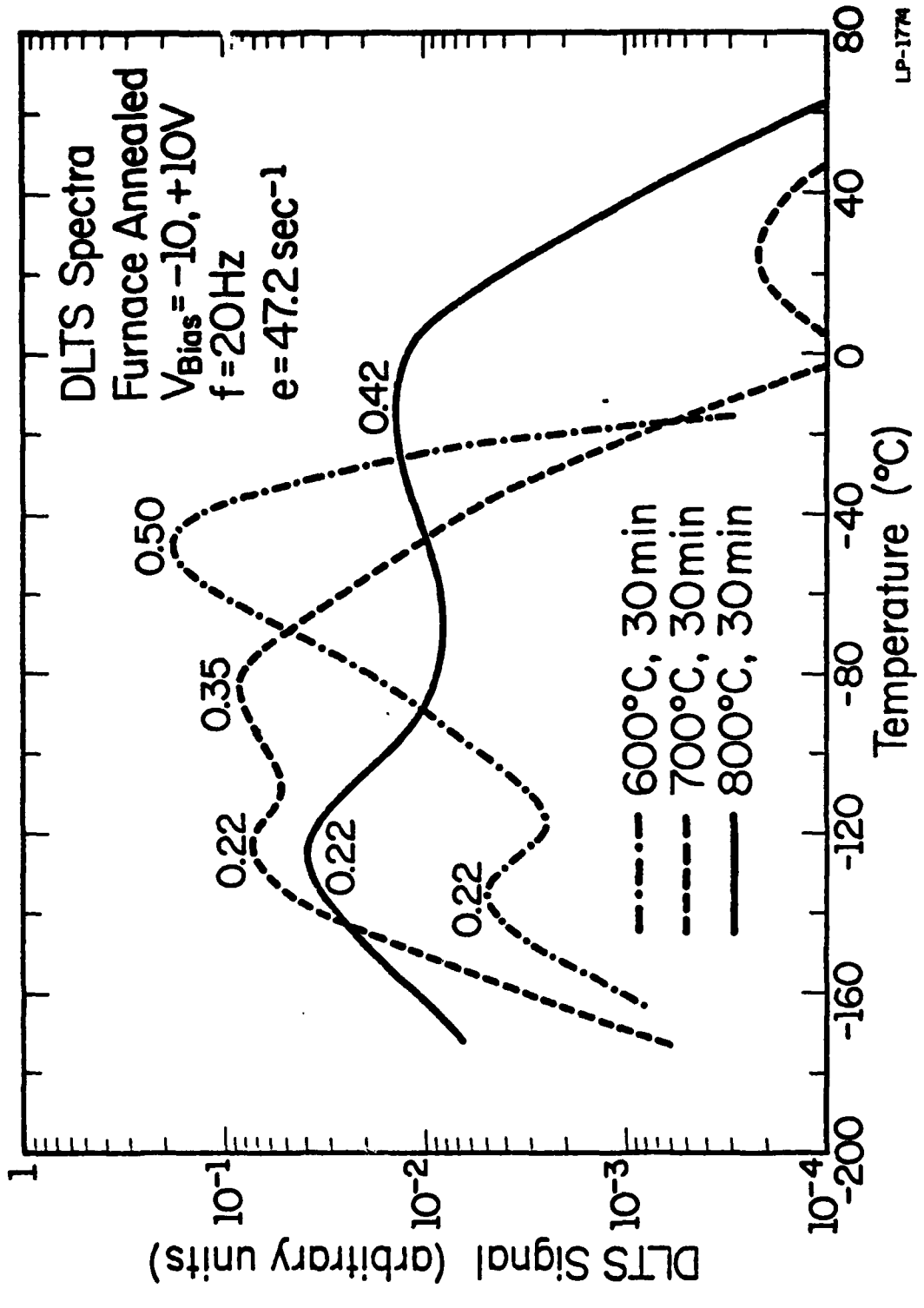


Fig. 3.1. DLTS spectra for Schottky barriers fabricated on furnace annealed material [33].

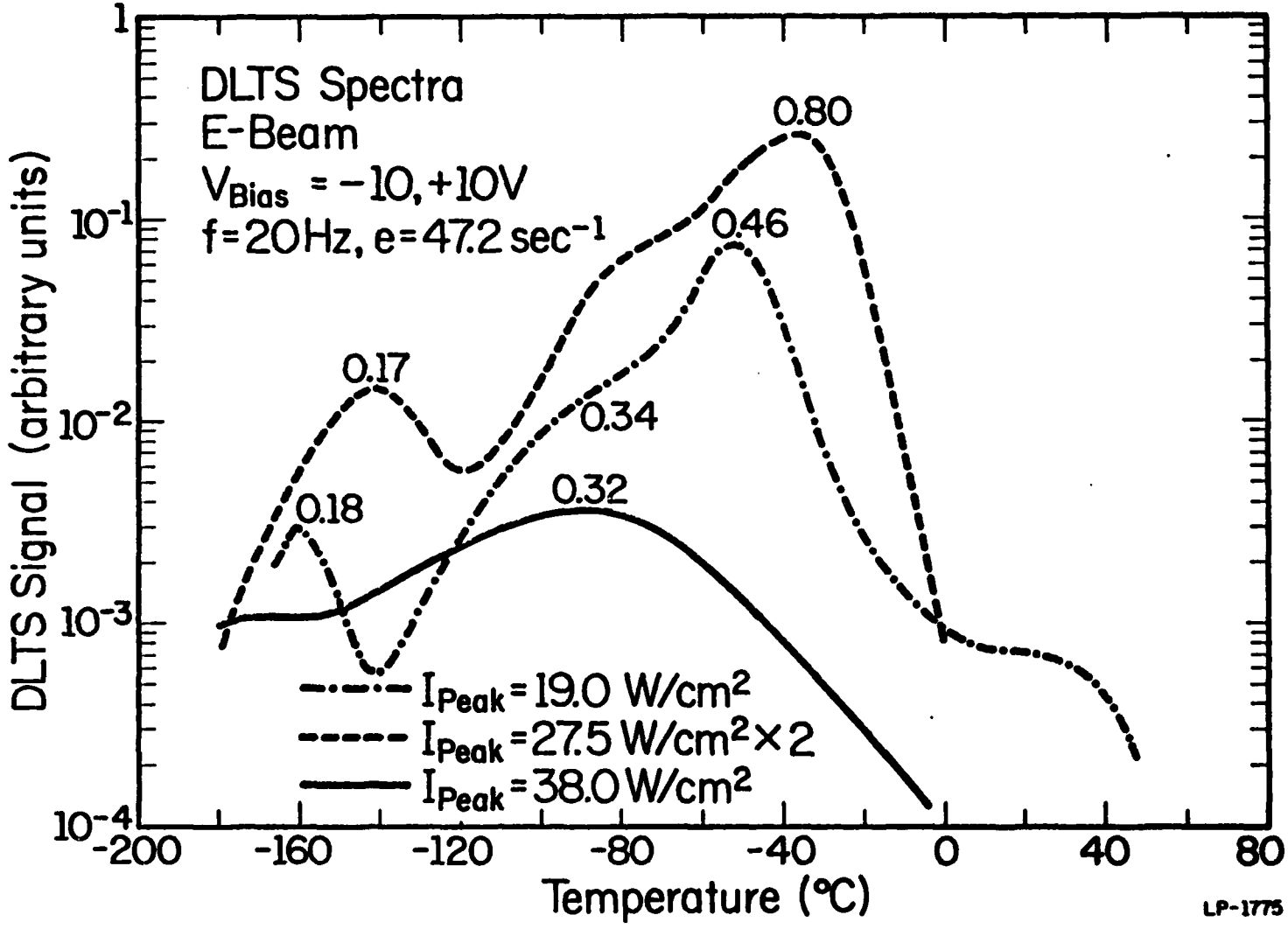


Fig. 3.2. DLTS spectra for samples fabricated on SLEB annealed material [33].

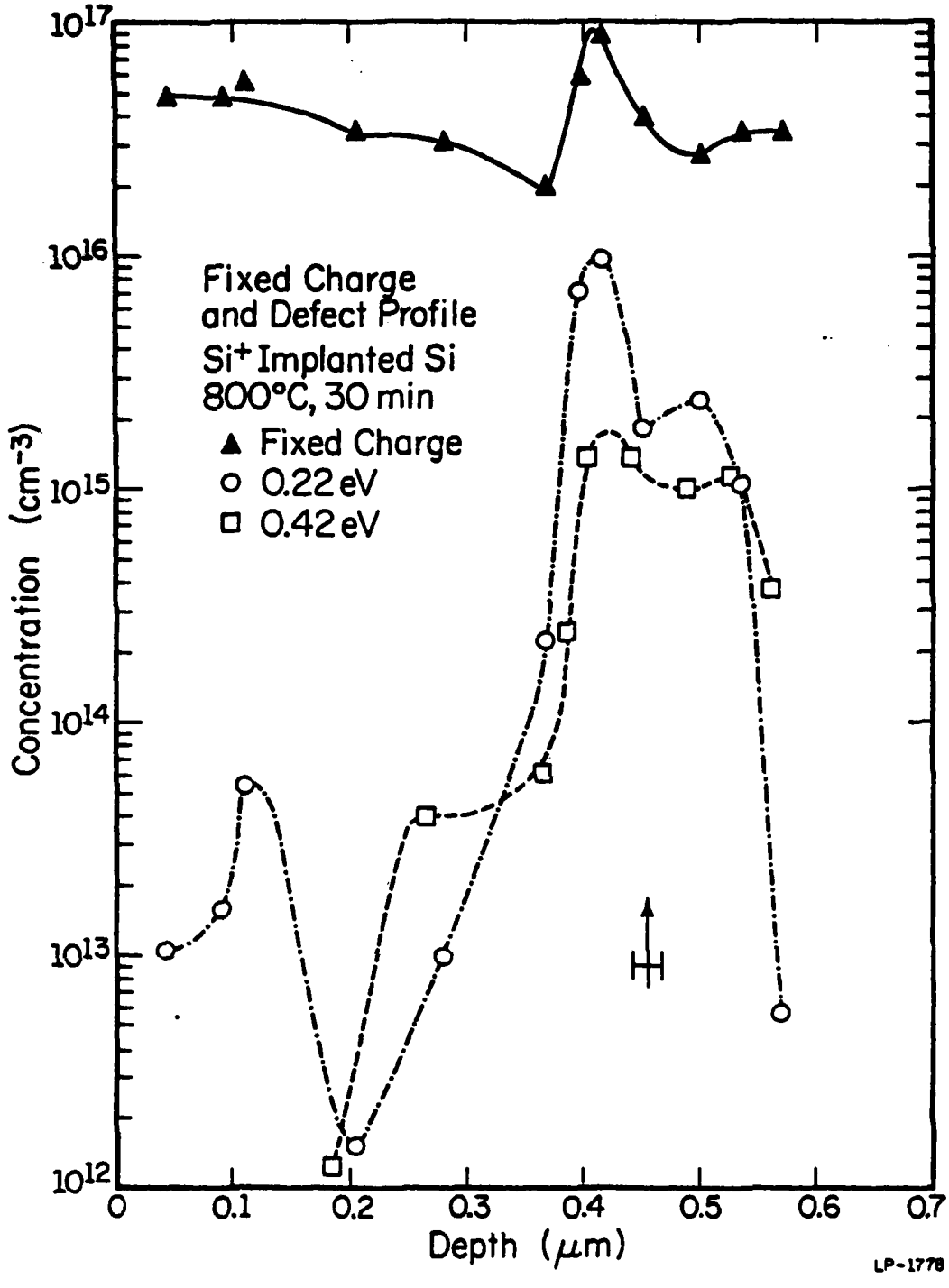


Fig. 3.3. Fixed charge and defect profiles for 800°C furnace annealed material [33].

arrow) and a relatively small concentration is observed in the near surface region. An apparent gettering effect occurs at the interface with the trap profile peak following that of the fixed charge.

The profile of fixed charge and defect concentrations for the 38 W/cm^2 SLEB annealed material is shown in Fig. 3.4. In this case, the residual defect level is small, thus fixed charge is defined as being due entirely to ionized donors. Unlike the 800°C case, very little dopant redistribution takes place and only a single defect signal appears, also at the original amorphous-crystalline interface. An improvement is also seen in the defect concentration. Peak concentrations are a factor of ten smaller than in the 800°C furnace case, while near surface defect densities are a factor of five to ten smaller.

3.2. Gallium Arsenide

The DLTS signal reflects traps in the n-side of the p^+-n junction due to the greater extension of the depletion region into the more lightly doped material. The thermally annealed samples have a breakdown voltage of 35 V and reverse saturations on the order of 10^{-12} A. Most of the SLEB samples have significantly higher breakdown voltages and lower reverse leakage currents.

The DLTS spectra for the p^+-n diode fabricated from 900°C, 30 minute thermally annealed n-GaAs displays four distinct peaks. Energy levels, ΔE= 0.22, 0.41, 0.47 and 0.77 eV below the conduction band edge are obtained from Arrhenius plots (Fig. 3.5). The deepest trap, ΔE = 0.77 eV is also the most prominent one. Defects with activation energies within $\pm$ 0.04 eV of the first three traps, E1 through E3 have been previously observed in implanted VPE n-GaAs (34), although the dominant peak at 0.83 eV is 7.7% in energy above

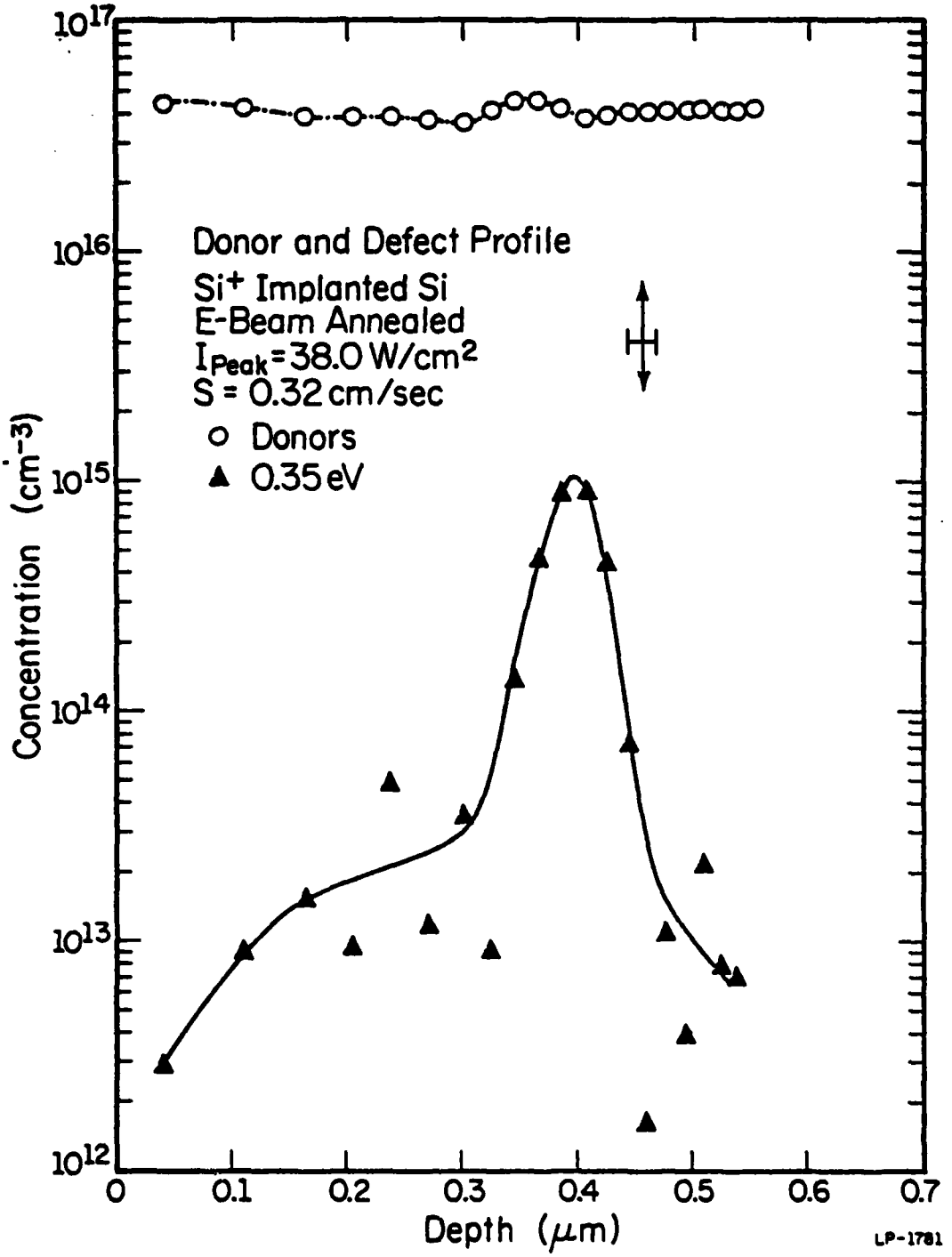


Fig. 3.4. Donor and defect profiles for 38.0 W/cm^2 SLEB annealed material [33].

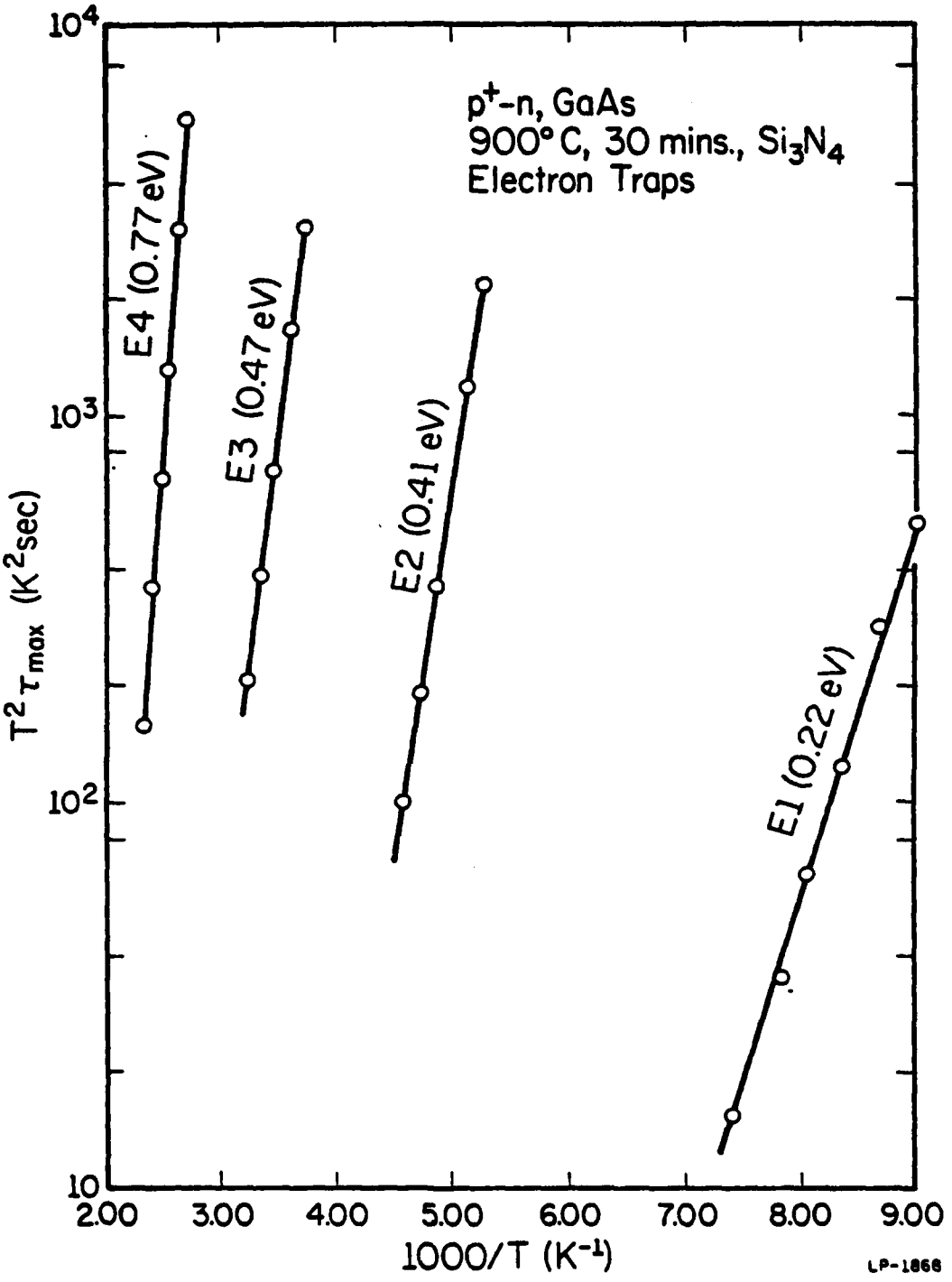


Fig. 3.5. Arrhenius plots for electron traps in p^+-n diodes fabricated on 900°C furnace annealed material.

the dominant level identified in that paper.

Three peaks appear in samples annealed with a 25 keV, 4.5 mA electron beam, but further analysis revealed a fourth near L2. Arrhenius plots for these peaks are shown in Fig. 3.6. Activation energies within $\pm$ 0.04 eV of the observed levels ΔE = 0.24 and 0.38 eV below the conduction band edge have been previously identified in implanted VPE n-GaAs (34), with the dominant peak occuring 10.8% in energy below the most prevalent signal seen in that earlier study.

The fixed charge and defect profiles for 900°C and SLEB annealed samples are shown in Fig. 3.7 and Fig. 3.8, respectively. In both cases, the electron trap profile reveals an extreme dip in concentration, reaching a minimum at roughly 0.7 μm below the junction for the 900°C device and 3.6 μm for SLEB. On the other hand, the fixed charge profiles differ considerably.

It has been observed that n-GaAs with carrier concentrations of 5×10^{16} cm^{-3} or less, which undergoes heat treatment $\geq$ 900°C followed by quenching, will become less n-type or be converted to p-type material (35). The thermal conversion results from the transfer of Si atoms from donor sites to acceptor sites through a trapping process during rapid quenching. This explains the shape of the fixed charge profile in Fig. 3.8, since the GaAs used in this study is doped with 8×10^{15} Si-cm^{-3} and is quenched during the SLEB process. By contrast, the 900°C sample is pulled slowly to avoid quenching, thus resulting in the relatively uniform profile given in Fig. 3.7.

The SLEB defect profile is expected to remain at the concentration level which has been reduced by thermal conversion but instead increases rapidly at approximately 4.3 μm. This anomaly can be interpreted as being due to the limitations of the Boonton 72B (37). The capacitance meter operates

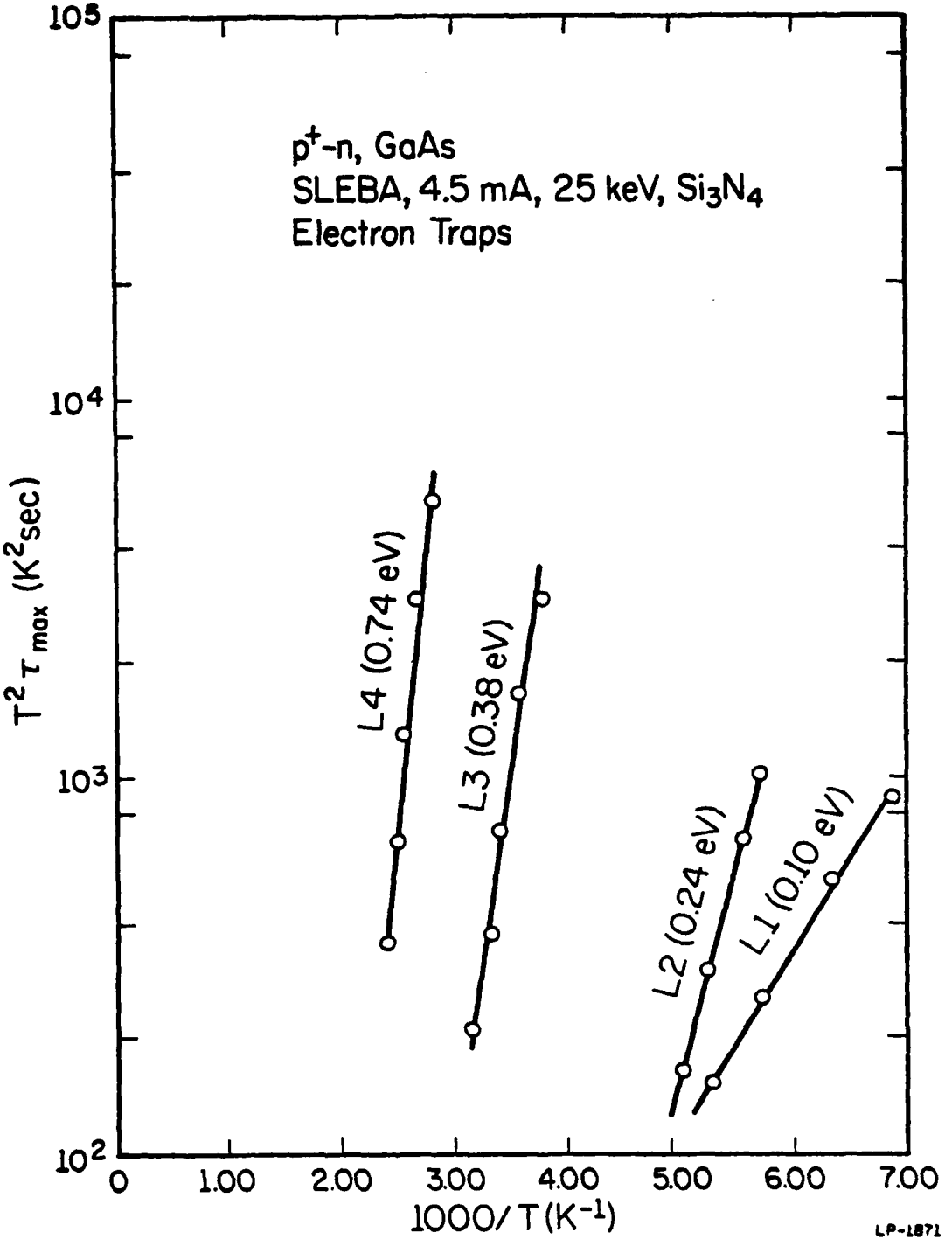


Fig. 3.6. Arrhenius plots for electron traps in p^+-n diodes fabricated on SLEB annealed material. L1 through L4 represent 4 defect levels.

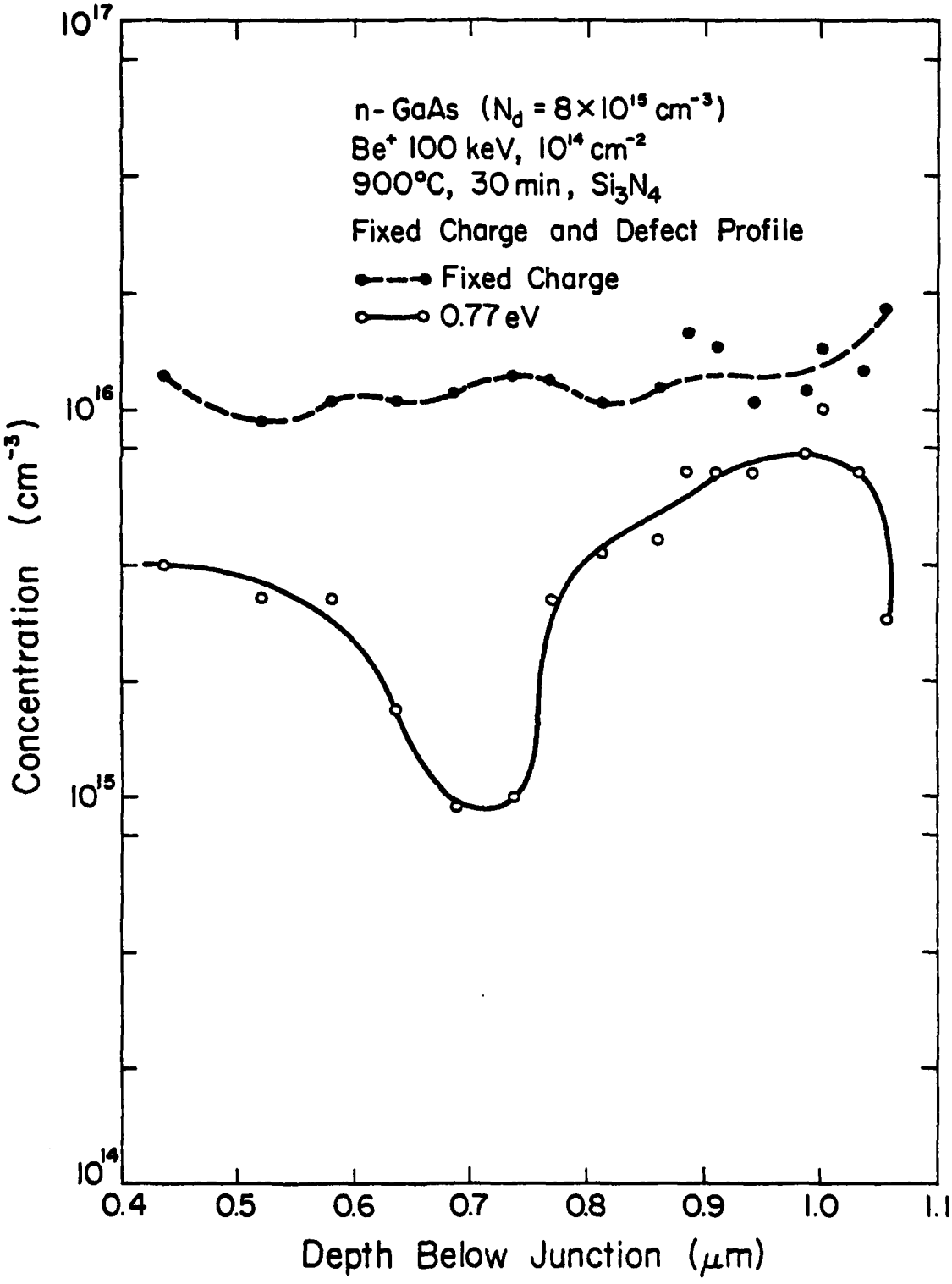


Fig. 3.7. Fixed charge and electron trap concentration profiles for samples annealed at 900°C for 30 minutes.

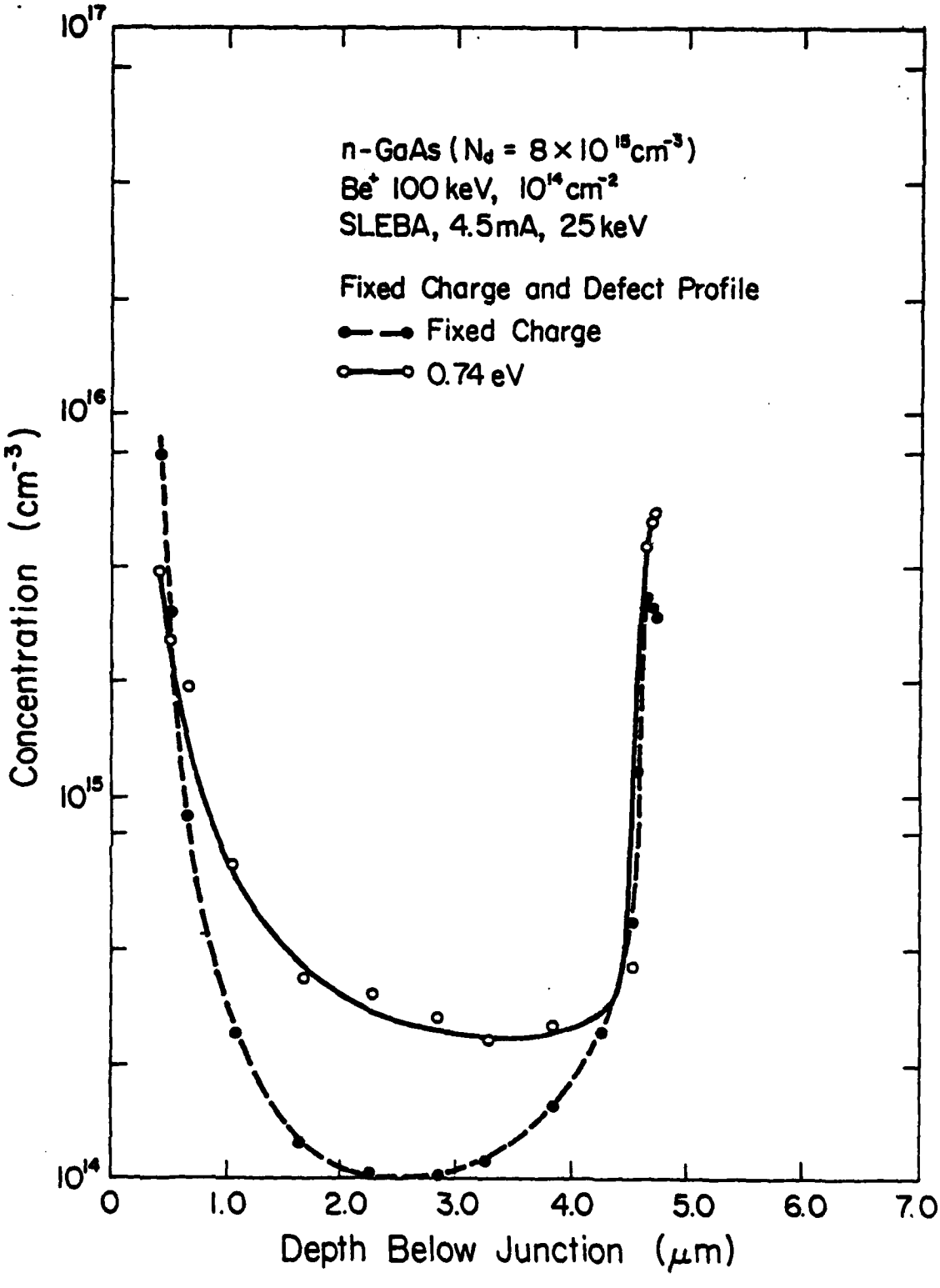


Fig. 3.8. Fixed charge and electron trap concentration profiles for samples SLEB annealed at 4.5 mA, 25 keV.

at a given Q point. With a large reverse bias, the leakage current increases to a point where the meter mistakes it for reactive current. This gives the appearance of a large capacitance and therefore larger trap concentrations. Fig. 3.9 illustrates the effect of C-V measurements taken with the Boonton72B on concentration using nitrogen free, undoped VPE GaP. The identical result occurs for large reverse bias as in this paper, though this phenomenon takes place at a higher applied voltage because of the sample purity.

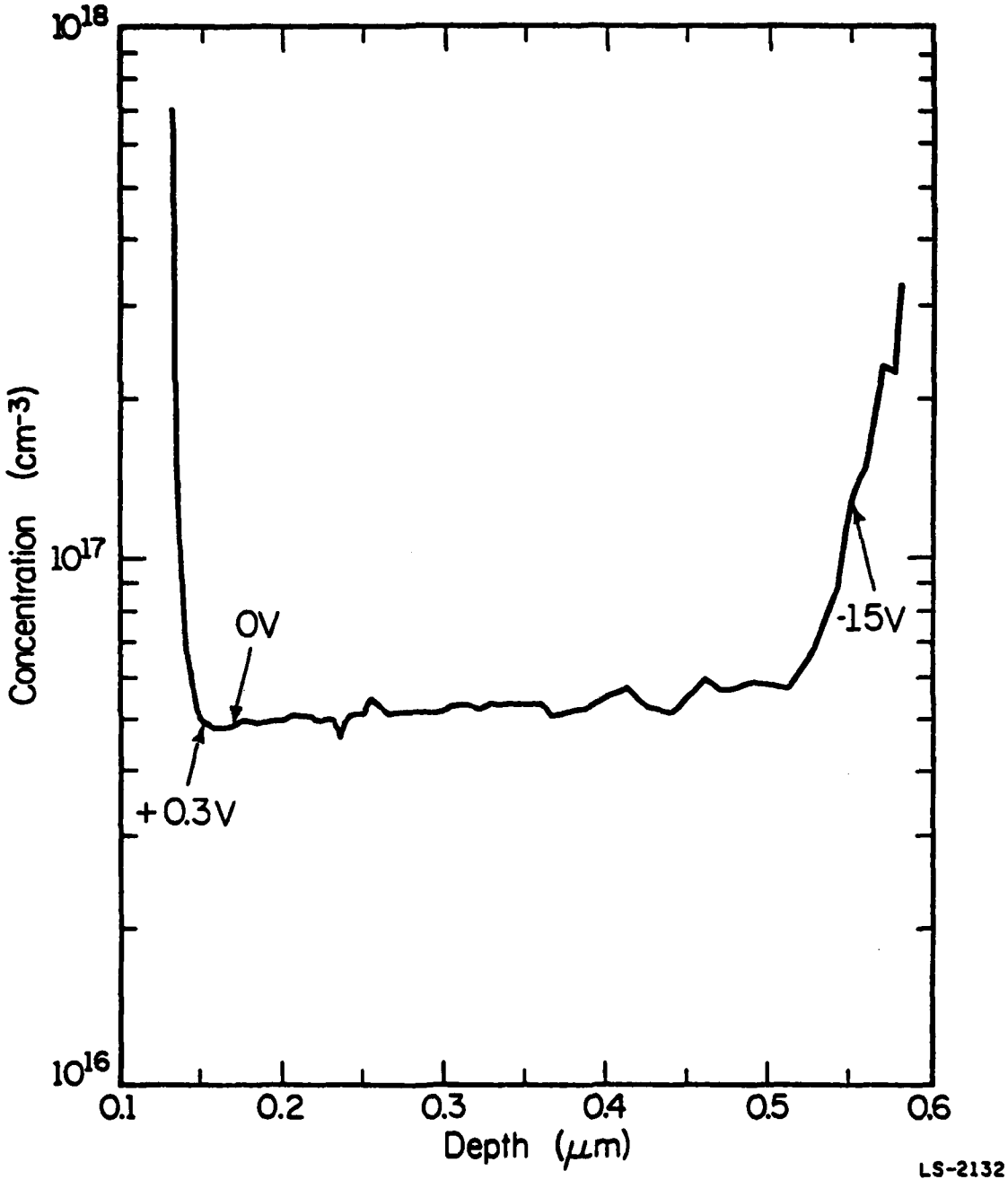


Fig. 3.9. Trap concentration of undoped VPE GaP material derived from C-V analysis [37].

4. CONCLUSION

We conclude from the results that SLEB annealing of Si is more effective than thermal annealing in reducing residual damage and limiting background dopand redistribution, but in GaAs the SLEB quenching effect poses a control problem because of thermal conversion. Further work is necessary to find methods of eliminating this quenching phenomenon. One suggestion is to preheat the mounting plate to just below sample melting point, passing the electron beam over the sample and then slowly cooling the plate. Heating and cooling times, though, must be carefully monitored since prolonged heating will effectively thermal anneal the samples thereby negating the advantages of SLEB annealing, and a cooling rate of approximately 150°C per minute is required to eliminate quenching.

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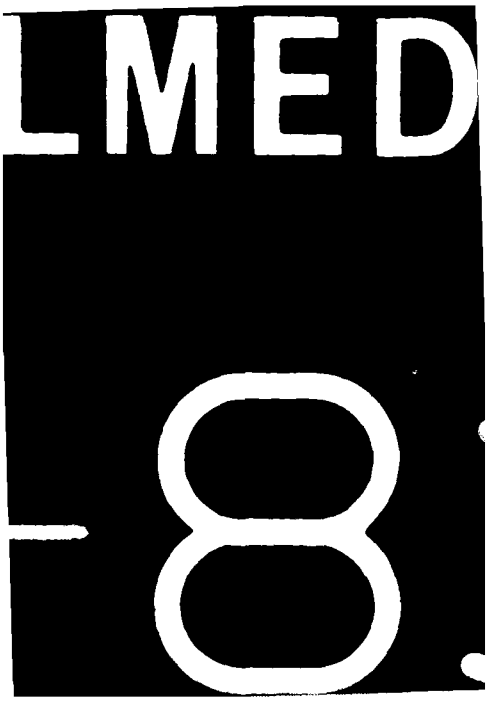
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